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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:	Docket No.: 550,685
James Wittman Babcock, et al.	Group Art Units: 3743
Serial No.: 10/625,051	Examiner: T. McKinnon
Filed: July 23, 2003	Date: July 6, 2005

FOR: METHOD OF EXTENDING THE OPERATIONAL PERIOD OF A HEAT EXCHANGER IN A CHIP TESTER

APPEAL BRIEF UNDER 37CFR 1.192 AND AUTHORIZATION TO PAY FEES

Mail Stop APPEAL BRIEF PATENTS
Commissioner for Patents
P.O. Box 1450
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Sir:

An appeal brief is hereby submitted, in triplicate, in the above-referenced case.

Please charge Deposit Account 19-3790 for any fees due with the filing of this appeal brief.

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TABLE OF CONTENTS

(1) REAL PARTY IN INTEREST

In the present case, the real party in interest is Unisys Corporation, a corporation of the State of Delaware, having principal offices at Township Line and Union Meeting Roads, Blue Bell, Pennsylvania 19424. An assignment to Unisys Corporation of the entire right, title and interest in the present invention is recorded in the U.S. Patent and Trademark Office at Real/Frame 014330/0683.

(2) RELATED APPEALS

No other appeals or interferences are known to the assignee, Unisys Corporation, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) STATUS OF CLAIMS

Independent claim 1 and dependent claims 2-13 are only active claims; and all of these claims are presently under a final rejection based on the last Office Communication that was mailed June 14, 2005.

(4) STATUE OF THE AMENDMENTS

In this case, no amendments have been filed. Instead, in response to a first office action in which all claims were rejected under 35USC103, a Request For Reconsideration was filed on 1/31/05. Then, in response to a second office action in which all claims were given a final rejection under 35USC103, another Request For Reconsideration was filed on 5/9/05. However, the Examiner maintained his rejection.

(5) SUMMARY OF INVENTION

The present invention is a method of extending the operational period of a heat-exchanger in a chip tester, where the heat-exchanger is of the type that includes an electric heater and a heat-sink that are joined together with a layer of attach material. Within the chip tester, the heat-exchanger is pressed against an integrated circuit chip to thereby maintain the chip's temperature near a set point while the chip is tested.

A prior art chip tester which has a heat-exchanger with an electric heater and a heat-sink that are joined together with a layer of attach material is disclosed in U.S. patent 5,821,505. For ease of reference, Fig. 1 of the `505 patent is reproduced herein as EXHIBIT "A" and labeled prior art. In that figure, reference numeral 11 identifies the integrated circuit chip which is to be tested while its temperature is maintained near the set point.

Also in Fig. 1, components 13 and 14 together comprise the heat-exchanger which maintains the chip's temperature near the set point. In that heat-exchanger, component 13 is a thin flat electric heater, and component 14 is a liquid cooled heat-sink. These components 13 and 14 are joined together by a thin layer of an attach material, which is too small to be shown in Fig. 1.

In Fig. 1, the chip 11 is tested by sending it the TEST-IN signals on the signal lines 12a, and by examining the chip's response via the TEST-OUT signals on the signal lines 12c. While that occurs, the power dissipation in the chip 11 varies because many transistors within the chip 11 turn-on and turn-off in response to

changes in the TEST-IN and TEST-OUT signals. As the power dissipation of the chip 11 increases the chip temperature tends to increase; and vise-versa.

A TEMP signal from the chip 11 in Fig. 1 is sent on signal line 12c to a power regulator 16 where it is compared to a SET-POINT signal on the signal line 12d. When the temperature of the chip 11 is too cold relative to the set point temperature, then the regular 16 increases the heater power P_h via a control signal CTL. Conversely, when the temperature of the chip 11 is too hot relative to the set point temperature, then the regulator 16 decreases the heater power P_h.

Due to the above described operation of the power regular 16, the testing of just a single chip typically subjects the heater 13 to thousands of different changes in temperature. Thus, as one chip after another are sequentially tested in the Fig. 1 chip tester over time, the total number of temperature changes to which the heater 13 is subjected can easily exceed one million.

The present inventors have closely analyzed the above temperature changes in the Fig. 1 tester to see if they have any long term adverse effect on the tester. What the present inventors found is that as the number of chips which have been tested increases, the thermal resistance increases through the attach layer which joins the heater 13 to the heat-sink 14. This attach layer is shown as item 102 in Fig. 18 of the `505 patent, and that figure is reproduced herein as Fig. 2 in EXHIBIT "B".

Further the present inventors have determined from their analysis that the above increase in thermal resistance is caused by microscopic stress cracks that are induced in the attach layer 102 when the heater 13 is

subjected to a large number of temperature changes while multiple chips 11 are tested. The occurrence of these stress cracks is not taught by the prior art, and these stress cracks are shown for the first time in Fig. 3 of the present patent application where they are indicated by reference numeral 200. That Fig. 3 is reproduced herein in EXHIBIT "C". The present inventors have determined that the stress cracks 200 occur because the heater 13 and the heat-sink 14 expand at different rates when the above temperature changes occur.

The presence of the stress cracks 200 is a serious problem because they eventually cause the thermal resistance through the attach layer 102 to become so large that the temperature of the chip 11 cannot be kept at the set point. When that occurs, the entire heat-exchanger (i.e. - the heater 13 and the attached heat-sink 14) needs to be removed from the tester and replaced. But replacing the entire heat-exchanger is expensive, and it also causes downtime on the chip tester.

After discovering the above cracks, the present inventors invented the process which is recited herein in claim 1. Initially in the process of claim 1, chips are tested in a manner which subjects the heat-exchanger to many temperature changes, all of which stay below the melting temperature of the layer of attach material between the electric heater and the heat-sink. Due to these temperature changes, the layer of attach material between the electric heater and the heat-sink remains solid, and stress cracks are eventually induced in that layer.

Next in the process of claim 1, the layer of attach material between the electric heater and the heat-sink is a subjected to a crack-healing temperature cycle in

which that layer is melted at least partially and re-solidified. Due to this step, all of the stress cracks in the layer of attach material are eliminated. Thereafter, in the process of claim 1, the heat-exchanger with the re-solidified crack-free layer of attach material is used again in the chip tester to test additional chips.

By the method of claim 1, the entire replacement cost of a new heat-exchanger is saved. In addition, by the method of claim 1, downtime on the chip tester is reduced because the time to remove one heat-exchanger and install another heat-exchanger greatly exceeds the time that it takes to subject the layer of attach material to the crack-healing temperature cycle of claim 1.

(6) ISSUES

In this appeal, there is only one issue; and that issue is stated below.

> Issue - Is claim 1 obvious or non-obvious, under 35USC103, based on the teachings of U.S. patent 5,869,176 (the `176 patent by Babcock et al.) and U.S. patent 5,930,893 (the `893 patent by Eaton).

The need to resolve the above issue by this appeal arises from 1) the second office action (mailed on 5/3/05) wherein all of claims 1-13 are given a final rejection under 35USC103 for being obvious based on the combined teachings of the `176 and `893 patents, and 2) the subsequent advisory action (mailed 6/14/05) wherein the final rejection was retained. Claim 1 is the only independent claim, so the remaining claims 2-13 are non-obvious if claim 1 is non-obvious.

(7) GROUPING OF CLAIMS

In this appeal, claim 1 is the only independent claim, and the remaining claims 2-13 are dependent on claim 1. To simplify the issue in this appeal, all of the claim 1-13 can stand or fall together based on whether claim 1 by itself is obvious or non-obvious.

(8) ARGUMENTS

Five major differences will now be pointed out between claim 1 and the cited prior art patents 5,864,176 and 5,930,893. For ease of reference to the language of claim 1, that claim is reproduced below.

> 1. A method of extending the operational period of a chip tester of the type that includes a heat-exchanger which has an electric heater and a heat-sink that are joined together with a layer of an attach material; said method including the steps of:
>
> testing chips in said chip tester in a manner that puts said heat-exchanger through multiple temperature changes where said layer stays in a solid state and where stress cracks are induced in said layer;
>
> subjecting said layer to a crack-healing temperature cycle in which said layer is melted at least partially and re-solidified; and thereafter,
>
> repeating said testing step.

First, claim 1 is limited to a method of achieving a particular end result in a chip tester. Specifically, claim 1 is limited to a "method of extending the operational period of a chip tester".

By comparison, in patent `176, no method of extending the operational period of any chip tester is

described. Instead, in patent `176, the only method which is described merely lowers the thermal resistance between two separate members that are not permitted to be joined together. This is achieved by placing a film of a liquid between the mating faces of the two separate members where the liquid is one that can subsequently be evaporated. See col. 12, line 43 to col. 13, line 33. There, one of the members is an integrated circuit chip 11 which is being tested and is not permitted to be joined to another member.

Similarly, in patent `893, no method of extending the operational period of any chip tester is described. Instead, in patent `893, the only method which is described merely eliminates voids between an electronic device and a heat-sink for that electronic device. These voids are eliminated by inserting a particular compound between the heat-sink and the electronic device, and then melting and solidifying the compound. Fig. 2 shows the voids at surfaces 110 and 210 which exist before the compound on a carrier 300 is melted, whereas Fig. 3 shows the voids at the surfaces 110 and 210 are eliminated after the compound on the carrier 300 has been melted. See line 53 of col. 3 to line 13 of col. 4.

Second, claim 1 is limited by requiring that "stress cracks" occur in a particular component of the chip tester. Specifically, these stress cracks must occur "in said layer" of attach material between an "electric heater" and a "heat-sink".

By comparison, in patent `176, no method is described where any cracks occur in a layer of attach material between an electric heater and a heat-sink. Instead, in patent `176, the only cracks which are described occur in an integrated circuit chip that is being

tested or an electrical conductor which carries signals to that chip. See col. 13 at lines 13-20.

Similarly, in patent `893, no method is described where any cracks occur in a layer of attach material between an electric heater and a heat-sink. Instead in patent `893, the only cracks which are described occur in a coating on an intermediate flexible insulator that is inserted between an electronic component and a heat-sink for that component. See col. 1 at line 38 to col. 2 at line 4.

Further in patent `893, there are no cracks "in" the layer 1000 which is shown in Figs. 2 and 3. Instead there are only "voids" in Fig. 2 which occur at the "surface" 110 of the heat-sink 100 and at the "surface" 210 of electronic component 200. These voids in Fig. 2 are not cracks; they are simply voids which occur because the surfaces of the items 100, 200, and 1000 are not perfectly smooth.

Third, claim 1 is limited to extending the operational period of the chip tester by inducing the stress cracks in the layer of attach material in a particular fashion. Specifically, the stress cracks are induced by putting "said heat-exchanger through multiple temperature changes".

By comparison, in patent `176, no method is described where any cracks are induced by multiple temperature changes. Instead, in patent `176, the only cracks that are described occur when "too much pressure is applied" to an integrated circuit chip that is being tested. See col. 13 at lines 13-20.

Similarly, in patent `893, no method is described where any cracks are induced by multiple temperature

changes. Instead, in patent `893, the only cracks that are described occur due to the absence of a "softener", such as "petroleum jelly", in a compound that joins a heat-sink to an electronic component. See col. 1 at line 58 to col. 2 at line 4.

Fourth, claim 1 is limited to extending the operational period of the chip tester by "healing" the "stress cracks" that are "in said layer". Specifically, the stress cracks "in" the layer of attach material between the electric heater and the heat-sink are healed by "subjecting said layer to a crack-healing temperature cycle".

By comparison, in patent `176, no method is described where any cracks are healed in any object. Instead in patent `176, the cracks in the chips that occur when "too much pressure is applied" are never healed. See col. 13 at lines 13-20. If those chips crack, they must simply be thrown away.

Similarly, in patent `893, no method is described where any cracks are healed in any object. Instead, in patent `893, the cracks that are described at line 58 of col. 1 to line 4 of col. 2 are simply avoided altogether by including a "softener" such as "petroleum jelly" in the compound that is coated onto a "intermediate flexible insulator".

Further, in patent `893, there are no "cracks" which are "in" any layer in Figs. 2 and 3 that are healed. Instead in Figs. 2 and 3, only the top and bottom surfaces of component 1000 are reshaped so that they match the uneven surface 110 of the heat-sink 100 and the uneven surface 210 of the semiconductor 200. This surface

reshaping eliminates the voids on the surfaces 110 and 210 that are shown in Fig. 2.

Fifth, claim 1 is limited to extending the operational period of a chip tester by requiring that the chip tester be used to test chips before the crack healing temperature cycle occurs and after the crack healing temperature cycle occurs. Specifically, this limitation is imposed by the sequence of the "testing" step, the "subjecting" step, and the "repeating" step.

By comparison, in patent `176, no method is disclosed where anything is used to perform a useful function before and after a crack healing step. Similarly, in patent `893, no method is disclosed where anything is used to perform a useful function before and after a crack healing step.

Based on the above five major differences between claim 1 and the cited prior art, it is respectfully submitted that claim 1, as a whole, is not obvious. The overall end result which is accomplished by the method of claim 1 (extending the "operational period" of a "chip tester") is different. The particular item which cracks in claim 1 (the "layer between the electric heater and the heat-sink") is different. The cause of the cracks in claim 1 (subjecting the heat-exchanger to "multiple temperature changes") is different. The "healing" of the "cracks" which are located "in" a "layer" (between the electric heater and the heat-sink) is different. And, the performing of a useful function (testing chips) before and after a crack healing step is different.

SIGNATURE

A request is hereby made for the Board in this appeal to reverse the Examiner and rule that the cited patents `176 and `893 do not make claim 1 obvious under 35USC103.

Respectfully submitted,

By _____
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Certificate of Mailing (37CFR 1.8a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief Patents, P.O. Box 1450, Alexandria, VA. 22313-1450.

Date: July 6, 2005

Patti S. Preddy
_____

APPENDIX (1-4)

WHAT IS CLAIMED IS:

1. A method of extending the operational period of a chip tester of the type that includes a heat-exchanger which has an electric heater and a heat-sink that are joined together with a layer of an attach material; said method including the steps of:

testing chips in said chip tester in a manner that puts said heat-exchanger through multiple temperature changes where said layer stays in a solid state and where stress cracks are induced in said layer;

subjecting said layer to a crack-healing temperature cycle in which said layer is melted at least partially and re-solidified; and thereafter,

repeating said testing step.

2. A method according to claim 1 wherein said crack-healing temperature cycle is performed while a spacer is in said heat-exchanger which remains solid and keeps the thickness of said layer constant.

3. A method according to claim 1 wherein said crack-healing temperature cycle is performed while said heat-exchanger is in said tester.

4. A method according to claim 1 wherein said crack-healing temperature cycle is performed after said heat-exchanger is removed from said tester.

5. A method according to claim 1 wherein said crack-healing temperature cycle includes the substep of sending an electric current to said electric heater with a magnitude and duration that causes said layer to melt at least partially.

6. A method according to claim 1 wherein said crack-healing temperature cycle includes the substep of transferring heat to said heat-exchanger from an external source, with a magnitude and duration that causes said layer to melt at least partially.

7. A method according to claim 1 wherein said crack-healing temperature cycle includes the substep of transferring heat to said heat-exchanger by passing a hot liquid through said heatsink, with a magnitude and duration that causes said layer to melt at least partially.

8. A method according to claim 1 wherein said heatsink is of a type that includes a passageway for carrying a liquid coolant, and said crack-healing temperature cycle includes the substep of preventing said coolant from moving through said passageway while said layer is melted at least partially.

9. A method according to claim 1 wherein said heatsink is of a type that includes a passageway for carrying a liquid coolant, and said crack-healing temperature cycle includes the substep of heating said coolant as it moves through said passageway while said layer is melted at least partially.

10. A method according to claim 1 wherein said crack-healing temperature cycle includes the substep of pressing against said electric heater with a member that simulates one of said chips in said testing step, while said layer is melted at least partially.

11. A method according to claim 1 wherein said crack-healing temperature cycle includes the substep of positioning said heater above said heatsink and having gravity force said heater towards said heatsink while said layer is melted at least partially.

12. A method according to claim 1 wherein said crack-healing temperature cycle includes the substep of pressing against said heater with a springy member while said layer is melted at least partially.

13. A method according to claim 1 wherein said crack-healing temperature cycle includes the substep of limiting lateral movement of said heater, relative to said heatsink, with a mechanical stop while said layer is melted at least partially.

EXHIBIT "A"

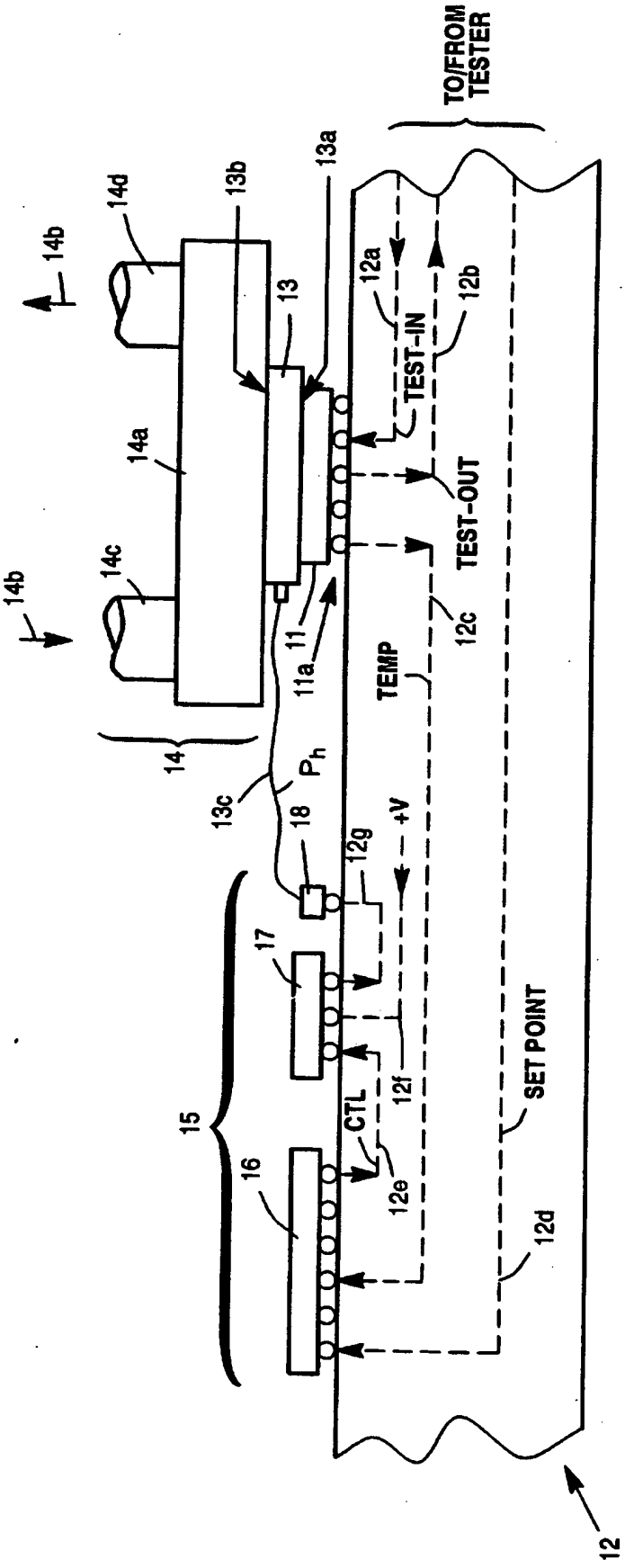

Figure 1

EXHIBIT "B"

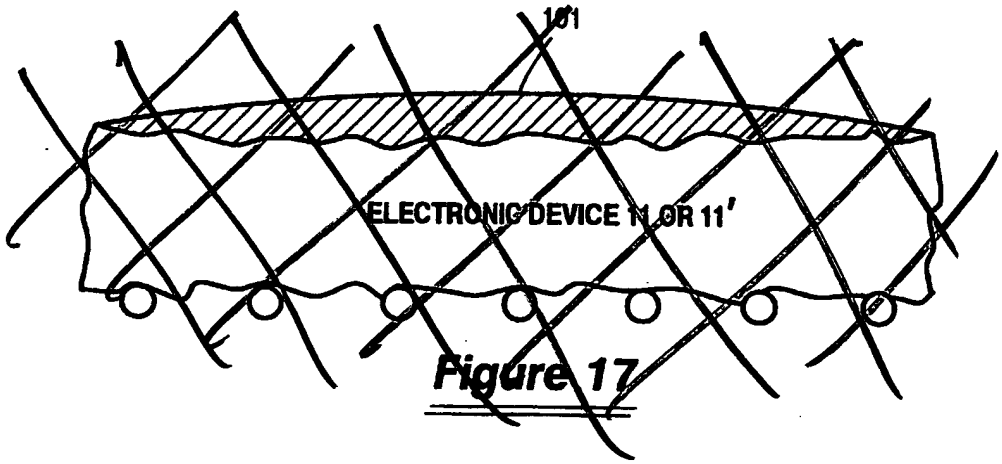

Figure 17

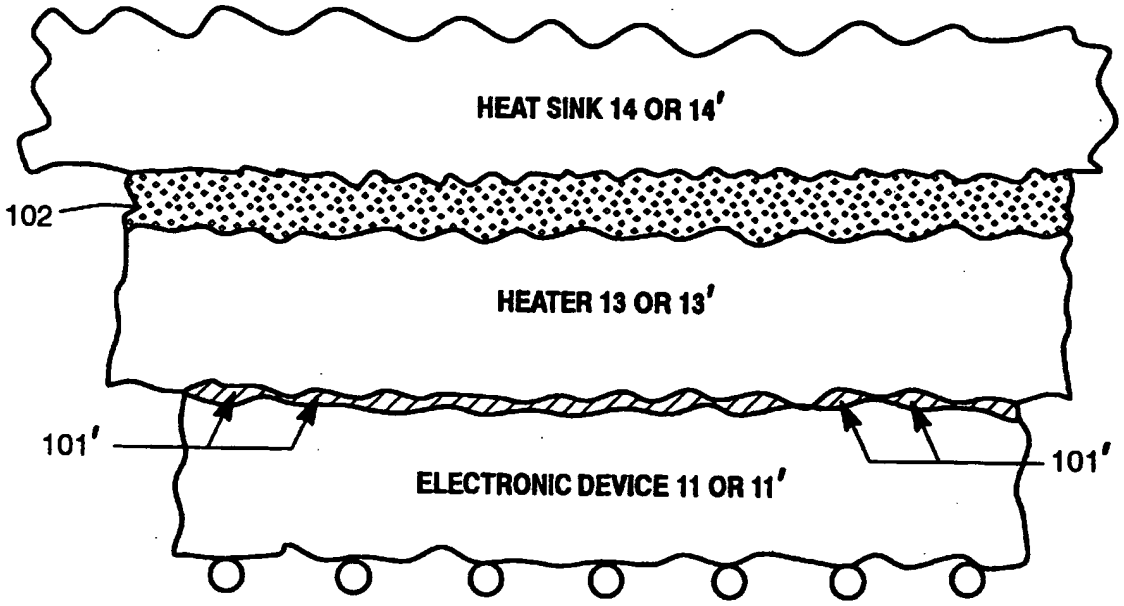

Figure 18

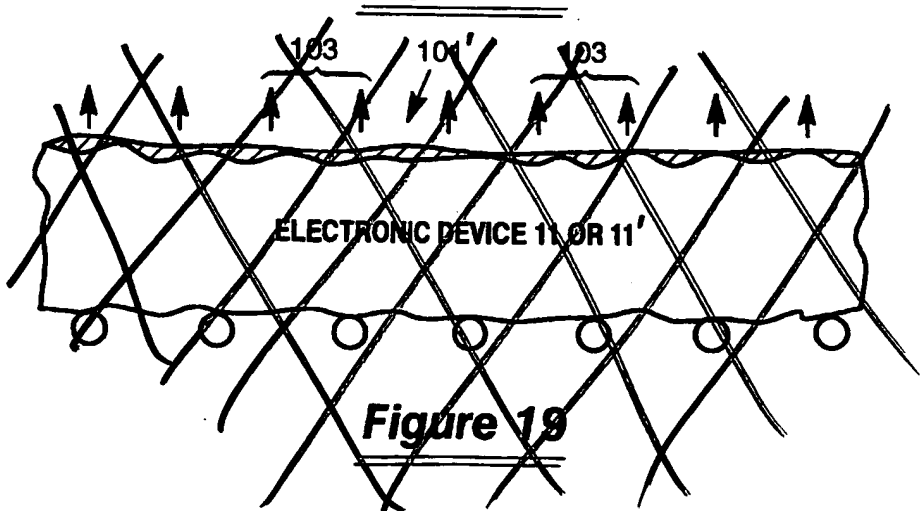

Figure 19

EXHIBIT "C"

FIG. 3